Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3081	(word adj lines) and (bit adj lines) and ONO	US-PGPUB; USPAT	OR	ON	2005/06/11 12:31
L2	808	1 and (nonvolatile adj memory)	US-PGPUB; USPAT	OR	ON	2005/06/11 12:31
L3	610	2 and (width or dimension)	US-PGPUB; USPAT	OR	ON	2005/06/11 12:47
L4	506	3 and plurality	US-PGPUB; USPAT	OR	ON	2005/06/11 12:32
L5	235	4 and @ad<"20020513"	US-PGPUB; USPAT	OR	ON	2005/06/11 13:08
L6	30	5 and (ONO same (width or dimension))	US-PGPUB; USPAT	OR	ON	2005/06/11 12:47
L7	33	(width with ONO) and (word adj line) and @ad<"20020513"	US-PGPUB; USPAT	OR	ON	2005/06/11 13:06
L8	28	7 not 6	US-PGPUB; USPAT	OR	ON	2005/06/11 13:08
L9	1	(width with ONO) and (word adj line)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/11 13:07
L10	4	(width same ONO) and (word adj line)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/11 13:08
L11	210	(width same ONO) and (word adj line)	US-PGPUB; USPAT	OR	ON	2005/06/11 13:15
L12	127	11 and @ad<"20020513"	US-PGPUB; USPAT	OR	ON	2005/06/11 13:15
L13	99	12 not 8	US-PGPUB; USPAT	OR	ON	2005/06/11 13:08
L14	334	((larger or wider or greater) same ONO) and (word adj line)	US-PGPUB; USPAT	OR	ON	2005/06/11 13:32
L15	199	14 and @ad<"20020513"	US-PGPUB; USPAT	OR	ON	2005/06/11 13:15
L16	172	15 not 13	US-PGPUB; USPAT	OR	ON	2005/06/11 13:15
L17	151	16 and bit	US-PGPUB; USPAT	OR	ON	2005/06/11 13:15
L18	4	((larger or wider or greater) same ONO) and (word adj iine)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/11 13:32

US-PAT-NO: 6448606

DOCUMENT-IDENTIFIER: US 6448606 B1

TITLE: Semiconductor with increased gate coupling coefficient

---------- KWIC ---------

Detailed Description Text - DETX (2):

Referring now to FIG. 1 (PRIOR ART), therein is shown a cross section of a conventional semiconductor memory device 100, such as a Flash EEPROM (electrically erasable programmable read only memory), in an intermediate state of processing. The structure shown is the result of a "bit-line" isolation technique called the "local oxidation of silicon" (LOCOS) isolation for making a floating gate. At this stage of processing, the floating gate for the semiconductor memory device 100 is shown on a semiconductor substrate 102, generally of doped silicon, with insulating field oxide (FOX) regions 104 and 105, a dielectric tunnel oxide (TOX) layer 106, a first polysilicon (poly) layer 108, an insulating oxynitride (ONO) layer 110, and a second poly layer 112 sequentially deposited on the semiconductor substrate 102. The **width** of the floating gates is given by W.sub.F, and the **width of the ONO** layer 110 between the control gates is W.sub.C with the **widths** being measured conformally along the respective surfaces.

Detailed Description Text - DETX (6):

Since the word line completely overlays the floating gates 108, the surface area that they couple is best described as W=the **width of the ONO** layer sandwiched between the two poly layers. ##EQU3## C.sub.TOX =Tunnel oxide capacitance C.sub.ONO =ONO capacitance A.sub.TOX =Surface area of tunnel capacitor A.sub.ONO =Surface area of ONO capacitor T.sub.TOX =Tunnel oxide thickness T.sub.ONO =ONO thickness

DOCUMENT-IDENTIFIER: US 20020012745 A1

TITLE: Flash memory and methods of writing and erasing the same as well as a method of forming the same

---------- KWIC ---------

Detail Description Paragraph - DETX (119):

[0177] An **ONO** film 31 is entirely formed and further a polysilicon 25 is deposited before a resist is used to pattern the polysilicon 25 into a stripe-shape in a longitudinal direction with a slightly **wider** than a lateral length of the trench in a plan of FIG. 36(a), thereby forming a control gate 5. Subsequently, the exposed **ONO** film 31 is etched to etch the polysilicon 24 to adjust the width in lateral direction, so that as can be seen from FIG. 36(b) and (c), floating gates 4 separated from each other are formed to finish the processes until FIG. 36. The control gate 5 in FIG. 36(c) is a stripe continuing in top and bottom directions in the drawing.

US-PAT-NO: 6552387

DOCUMENT-IDENTIFIER: US 6552387 B1

TITLE: Non-volatile electrically erasable and programmable semiconductor memory cell utilizing asymmetrical charge trapping

---------- KWIC ---------

Brief Summary Text - BSTX (17):

A single transistor **ONO** EEPROM device is disclosed in the technical article entitled "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," T. Y. Chan, K. K. Young and Chenming Hu, IEEE Electron Device Letters, March 1987. The memory cell is programmed by hot electron injection and the injected charges are stored in the oxide-nitride-oxide (**ONO**) layer of the device. This article teaches programming and reading in the forward direction. Thus, as in Mitchell, a **wider** charge trapping region is required to achieve a sufficiently large difference in threshold voltages between programming and reading. This, however, makes it much more difficult to erase the device.

US-PAT-NO: 6455888

DOCUMENT-IDENTIFIER: US 6455888 B1

TITLE: Memory cell structure for elimination of oxynitride (ONO) etch residue and polysilicon stringers

---------- KWIC ---------

Brief Summary Text - BSTX (11):

After application of the **ONO** layer 40, the poly II layer 44 is laid down over the **ONO** layer 40 as shown in FIG. 6a. Like the **ONO** layer 40, the poly II layer 44 also includes undulations as a result of the gaps 42 between rows of the poly I layer 38. The gaps 42 result in the poly II layer 44 being undulated such that portions of the poly II layer 44 adjacent an edge of a respective poly I layer row 38 (where the **ONO** layer 40 is thickest) is **greater** in height with respect to the substrate surface 30 than a portion of the poly II layer 44 which lies relatively over other areas. As will be discussed in **greater** detail below, the gaps 42 may lead to discontinuity in **ONO** 40 and poly II 44 thickness and even possibly film cracks or breaks.

Brief Summary Text - BSTX (12):

FIG. 6b illustrates a substantially large maximum step height (y.sub.M) that results because of the undulating poly II layer 44. In particular, the step height of a portion of the poly II layer that lies respectively over a poly I layer row 38 has a step height of y.sub.1, and a portion of the poly II layer that lies respectively over the gap 42 between adjacent poly I layer rows has a step height of y.sub.2. However, the portion of the poly II layer 44 which represents an undulation (i.e., the transition from the poly II layer lying over the poly I layer row 38 and over the gap 42 between poly I layer rows 38) has a step height of y.sub.M, where y.sub.M is substantially **greater** in height y.sub.1 or y.sub.2 and results in problems relating to overetch requirements and the formation of an **ONO** fence as will be discussed in **greater** detail below.

Brief Summary Text - BSTX (14):

FIG. 8 is a partial cross-sectional view of the memory device 10 taken at the portion 54. As is seen, the poly II layer 44 has been etched away leaving an **ONO** layer 40 laid down atop and along vertical sidewalls of the poly I layer 38. The field oxide 34 and tunnel oxide 36 of the substrate 30 are not shown for ease of understanding. In FIG. 9, the **ONO** layer 40 is shown being

substantially etched away using conventional etching techniques. The ONO layer 40 has a substantially **greater** step height at side wall portions 60 of the poly I layer 38. As a result, these side wall portions of ONO do not become completely etched away and leave what is coined an ONO fence 64 (FIG. 10) along the sidewalls of the poly I layer 38.

Detailed Description Text - DETX (6):

The exposed portions 136a, 136b and 136c (collectively referred to by reference numeral 136) of the poly I layer 120 will be transformed into insulating material (e.g., silicon dioxide) as will be discussed in **greater** detail below. The exposed portions 136 will be etched away to leave gaps having gradually sloping sidewalls which will isolate floating gates of adjacent memory cells. As noted above, such isolating was conventionally achieved by etching of the poly I layer to form gaps having steep sidewalls between floating gate lines. However, such etching of the poly I layer contributed to the formation of poly stringers because subsequently deposited ONO was not of uniform thickness. After an ONO etch was performed, areas of thicker ONO were not completely etched away and resulted in formation of an ONO fence which could lead to the formation of poly stringers. In the present invention, such open gaps between. adjacent floating gate lines do not have steep sidewalls but rather gently sloping walls so that subsequently deposited ONO will have a substantially uniform thickness (ie., thickness of the ONO is defined as the depth of the ONO perpendicular to the wafer surface) and is more readily etched. Thus, formation of an ONO fence is mitigated which in turn mitigates formation of poly stringers.

US-PAT-NO: 6366501

DOCUMENT-IDENTIFIER: US 6366501 B1

TITLE: Selective erasure of a non-volatile memory cell of a flash memory device

---------- KWIC ---------

Brief Summary Text - BSTX (7):

An example of a single transistor Oxide-Nitrogen-Oxide (**ONO**) EEPROM device is disclosed in the technical article entitled "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," T. Y. Chan, K. K. Young and Chenming Hu, IEEE Electron Device Letters, March 1987. The memory cell is programmed by hot electron injection and the injected charges are stored in the oxide-nitride-oxide (**ONO**) layer of the device. This article teaches programming and reading in the forward direction. Thus, a **wider** charge trapping region is required to achieve a sufficiently large difference in threshold voltages between programming and reading. This, however, makes it much more difficult to erase the device.

US-PAT-NO: 6317360

DOCUMENT-IDENTIFIER: US 6317360 B1

TITLE: Flash memory and methods of writing and erasing the same as well as a method of forming the same

---------- KWIC ---------

Detailed Description Text - DETX (120):

An **ONO** film 31 is entirely formed and further a polysilicon 25 is deposited before a resist is used to pattern the polysilicon 25 into a stripe-shape in a longitudinal direction with a slightly **wider** than a lateral length of the trench in a plan of FIG. 36(a), thereby forming a control gate 5. Subsequently, the exposed **ONO** film 31 is etched to etch the polysilicon 24 to adjust the width in lateral direction, so that as can be seen from FIGS. 36(b) and (c), floating gates 4 separated from each other are formed to finish the processes until FIG. 36. The control gate 5 in FIG. 36(c) is a stripe continuing in top and bottom directions in the drawing.

US-PAT-NO: 5933729

DOCUMENT-IDENTIFIER: US 5933729 A

TITLE: Reduction of ONO fence during self-aligned etch to eliminate poly stringers

---------- KWIC ---------

Brief Summary Text - BSTX (18):

According to one aspect of the present invention, a new **ONO** etch recipe is utilized which exhibits a substantially **greater ONO**-to-polysilicon selectivity. Consequently, a longer overetch of the **ONO** layer may be conducted without substantially impacting the underlying polysilicon. The overetch reduces the height of the **ONO** fence and thereby reduces its lateral shielding of polysilicon. The reduced lateral shielding prevents the formation of poly stringers during a subsequent etch of the polysilicon.

Detailed Description Text - DETX (4):

FIG. 8a illustrates a non-ideal anisotropic polysilicon etch profile 80 having an etched **ONO** layer which results in an angled **ONO** fence 82. The angled **ONO** fence 82 has a height "H" that spans a lateral distance "L" based on the angle .theta. of the non-ideal anisotropic etch profile. For any given etch profile, the longer the lateral distance "AL" the **ONO** fence 82 extends, the **greater** the possibility of poly stringer formation in the regions 84 and 86 due to the shielding of the polysilicon material 84 beneath the angled **ONO** fence 82 (called polyl stringers). The lateral distance "L"may be calculated by the formula:

Detailed Description Text - DETX (6):

Furthermore, as illustrated in FIG. 8c, this relationship between the height "H" and lateral distance "L" of the angled **ONO** fence 82 for a given profile .theta.' (wherein .theta.'=180.degree.-.theta.) also holds for non-ideal anisotropic profiles that are **greater** than 90.degree.. When .theta.'>90.degree., an etch profile 90 is achieved. Although the polysilicon 92 within the **ONO** fence 82 will be completely etched away during the SAE, the polysilicon (not shown) which previously overlaid the **ONO** layer (the second polysilicon layer that forms the control gate as will be discussed in **greater** detail infra) will be shielded by the **ONO** fence 82 and cause poly2 stringers in the regions 94 and 96.

Detailed Description Text - DETX (18):

According to one embodiment of the present invention, the high selectivity **ONO**-to-polysilicon etch includes a CF.sub.4 CHF.sub.3 0.sub.2 etch chemistry, wherein the CF.sub.4 has a volumetric flow rate of about 40 sccm, the CHF.sub.3 has a flow rate of about 15 sccm and the O.sub.2 has a flow rate of about 10 sccm. The gas combination is excited in a chamber to form a plasma, wherein the chamber pressure is about 25 mTorr and the excitation power is about 170 W. Although the above etch conditions are preferred, it should be understood that the high selectivity **ONO** etch is not limited to the above etch recipe, but rather contemplates any etch recipe that provides a substantially **greater** **ONO**-to-polysilicon selectivity than the prior art, that is, a selectivity **greater** than about 1:1.

Detailed Description Text - DETX (20):

The reduced **ONO** fence 126 is illustrated in its macroscopic context in FIG. 9j. Note that most of the **ONO** layer 110 having a thickness of about 120 Angstroms is removed, however, the regions 126 that overlie the steps of the first polysilicon regions 106a and 106b remain. These regions, which originally (before the SAE) had a substantially **greater** thickness than 400 Angstroms, constitute the reduced height **ONO** fence.

Detailed Description Text - DETX (24):

After delineating the word lines at step 204, a self-align etch (SAE) process is employed at step 206 to remove the first polysilicon layer and the overlying **ONO** layer in the regions between the desired word lines. The SAE 206 is a two step process in which the first step 206a includes performing a high selectivity insulator etch. The etch exhibits a substantially **greater** insulator-to-polysilicon selectivity than the prior art, thereby allowing an overetch to substantially reduce the height of the insulative fence without substantially impacting the underlying polysilicon. The second step 206b includes an anisotropic polysilicon etch to complete the defining of the word lines. Since the reduced insulative fence formed at step 206a does not substantially shield any polysilicon, the polysilicon etch of step 206b removes the polysilicon without any poly stringers left behind. After the SAE of step 206 the word lines are fully defined. Subsequent processing is then performed to form the source and drain regions in the substrate as is well known by those skilled in the art.